NIPPON PRECISION CIRCUITS INC.

SM9502A

Radio Controlled clock Receiver IC

OVERVIEW

The SM9502A is a BiCMOS RCC*1 receiver IC. It accepts low frequency standard wave input received from an external antenna, amplifies it, detects the data signal, and outputs a digital time code signal. Low-voltage operation is available, so that it can be used for the system operating with a 1.5V battery or a solar battery.

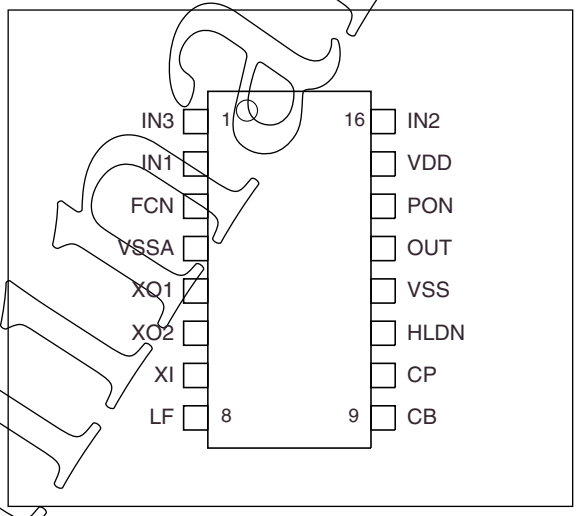
*1: Radio controlled clock

FEATURES

- Operating supply voltage range: 1.2 to 2.8V
- Operating current consumption: 36µA (typ) @1.5V
- Standby current consumption: 0.1µA (max) @1.5V
- High sensitivity: 0.3µVrms (typ) input (40kHz/60kHz input frequency)
- Low frequency standard wave range: 35kHz to 80kHz
- Include analog switch for antennatuning capacitors change
- AGC gain hold function
- External crystal filter connection
- BiCMOS process
- Package:16-pin VSOP, Chip form

PINOUT

(Top view)

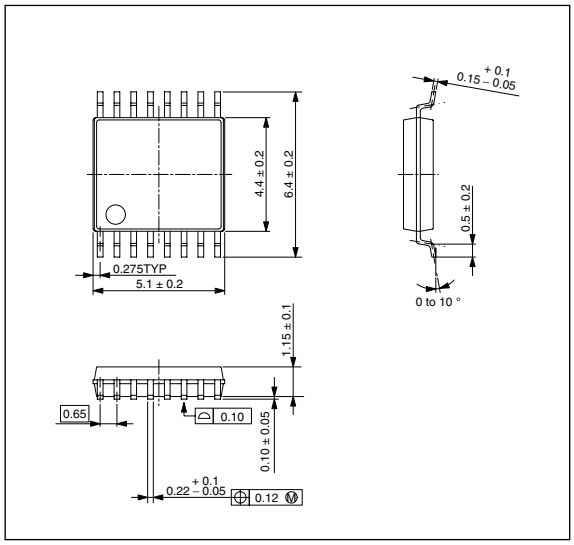


ORDERING INFORMATION

Device	Package
SM9502AV	16-pin VSOP
CF9502A	Chip form

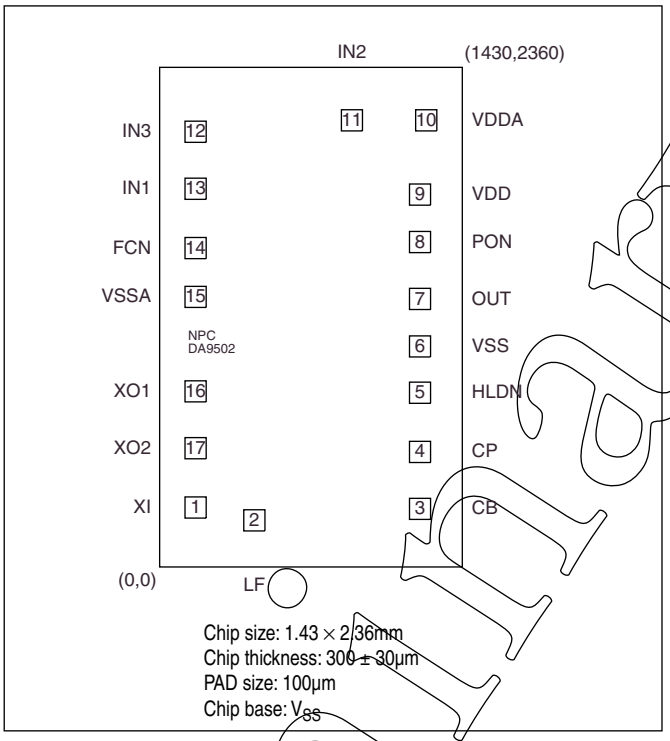
PACKAGE DIMENSIONS

(Unit: mm)



PAD LAYOUT

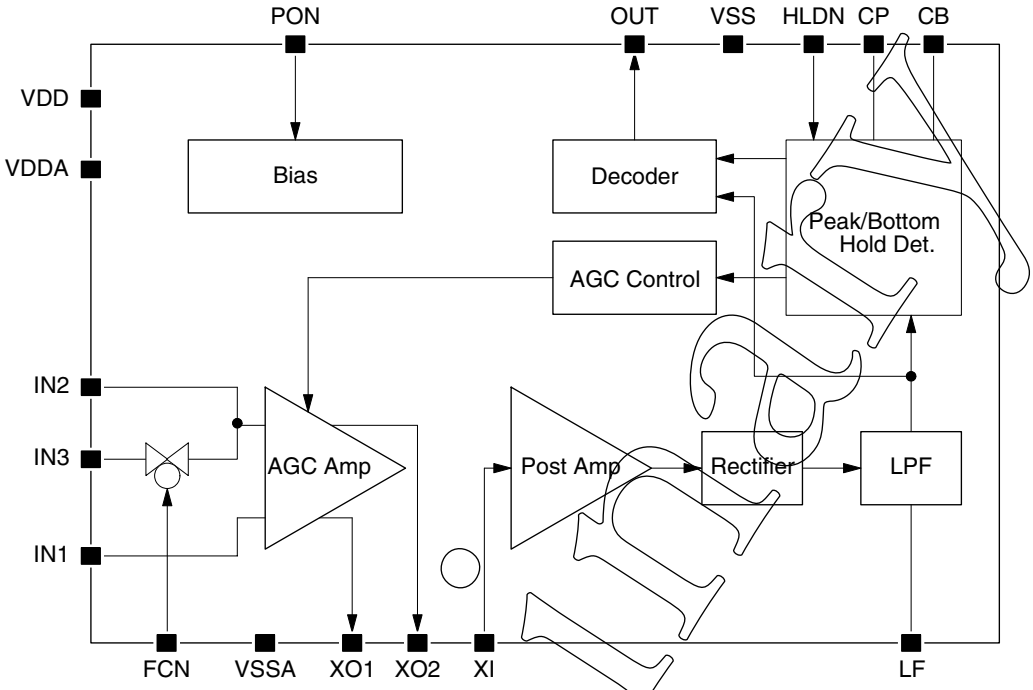
(Unit: µm)



PAD NAME and DIMENSIONS

Pad number	Pad name	Pad dimensions [µm]	
		X	Y
1	XI	170	280.6
2	LF	447.5	220
3	CB	1230	274.2
4	CP	1230	543.2
5	HLDN	1230	823.4
6	VSS	1230	1042
7	OUT	1230	1266.2
8	PON	1230	1535.2
9	VDD	1230	1759.4
10	VDDA	1259.4	2110
11	IN2	908.4	2110
12	IN3	170	2055.8
13	IN1	170	1786.8
14	FCN	170	1506.6
15	VSSA	170	1276
16	XO1	170	829.8
17	XO2	170	560.8

BLOCK DIAGRAM



PIN DESCRIPTION

Pad number	Pin number	Name	I/O[1]	A/D[2]	Description
1	7	XI	I	A	Crystal filter input connection
2	8	LF	O	A	Rectifier LPF capacitor connection
3	9	CB	O	A	Bottom-hold detector capacitor connection
4	10	CP	O	A	Peak-hold detector capacitor connection
5	11	HLDN	Ipu	D	AGC gain hold control (active LOW)
6	12	VSS	–	A	(–) Negative supply input (substrate potential)
7	13	OUT	O	D	Time code output (active LOW)
8	14	PON	Ipu	D	Standby-mode control input (active LOW)
9	15	VDD	–	A	(+) Positive supply input
10	–	VDDA	–	A	(+) Positive supply input (AGC amplifier)
11	16	IN2	I	A	Antenna input 2 (analog switch output)
12	1	IN3	I	A	Antenna input 3 (analog switch input)
13	2	IN1	I	A	Antenna input 1 (direct input)
14	3	FCN	Ipu	D	Analog switch control input (active LOW)
15	4	VSSA	–	A	(–) Negative supply input (AGC amplifier)
16	5	XO1	O	A	Crystal filter output 1
17	6	XO2	O	A	Crystal filter output 2

1. I: input, O: output, Ipu: input with pull-up resistor, –: supply pin
2. A: analog signal, D: digital signal

SPECIFICATIONS

Absolute Maximum Ratings

V_{SS} = 0V

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	V_{DD}		– 0.3 to 7.0	V
Input voltage range	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Power dissipation	P_D	16-pin VSOP	150	mW
Storage temperature range	T_{stg}	16-pin VSOP	– 55 to 125	°C
		Chip form	– 65 to 150	°C

Recommended Operating Conditions

V_{SS} = 0V

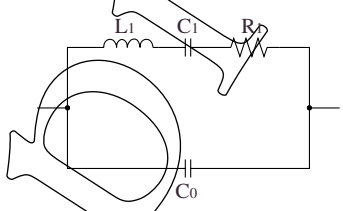
Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	V_{DD}		1.2 to 2.8	V
Operating temperature range	T_{opr}		– 20 to 70	°C

Electrical Characteristics

V_{DD} = 1.2 to 2.8V, V_{SS} = 0V, Ta = – 20 to 70°C unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Operating supply voltage	V_{DD}		1.2	–	2.8	V
Maximum operating current consumption[1]	I_{DDM}	V_{DD} = 1.5V, Ta = 25°C, no input signal, PON: VSS, OUT: Open	–	50	80	µA
Normal operating current consumption[1]	I_{DDT}	V_{DD} = 1.5V, Ta = 25°C, 0.1mVrms input amplitude (differential input), 500ms pulsewidth, PON: VSS, OUT: Open	–	36	–	µA
Standby mode current consumption	I_{ST}	PON, FCN, HLDN: VDD or Open	–	–	0.1	µA
Minimum input voltage range	V_{FMIN}	IN1–IN2 differential input, F_{IN} = 40kHz, 60kHz	–	0.3	1.0	µVrms
Maximum input voltage range	V_{FMAX}	IN1–IN2 differential input, F_{IN} = 40kHz, 60kHz	80		–	mVrms
Input frequency	F_{IN}	IN1–IN2 differential input	35	–	80	kHz
Analog switch resistance	R_A	V_{IN2} = 0V, V_{IN3} = 50mV	–	–	20	Ω
Startup time (at power-ON)[2]	t_{ON}		–	–	8	sec
Startup time (PON control)[2]	t_{PON}		–	–	8	sec
Input voltage	V_{IL}	PON, FCN, HLDN	–	–	0.2	V
	V_{IH}	PON, FCN, HLDN	V_{DD} – 0.2	–	–	V
Input current	I_{IL}	V_{IN} = 0V, PON, FCN, HLDN	– 1	–	–	µA
	I_{IH}	V_{IN} = V_{DD}, PON, FCN, HLDN	–	–	0.1	µA
Output voltage	V_{OL}	I_{OL} = 5µA, OUT	–	–	0.2	V
	V_{OH}	I_{OH} = – 5µA, OUT	V_{DD} – 0.2	–	–	V
Gain hold time	t_{HLD}	≤ ± 3dB variation	1	–	–	sec
Fall time output propagation delay[3]	t_{DN}	FIN = 40/60kHz, standard crystal, NPC standard jig	–	–	160	ms
Rise time output propagation delay[3]	t_{UP}		–	–	200	ms
LOW-level output pulsewidth[4] (200ms)	T_{200}		100	200	300	ms
LOW-level output pulsewidth[4] (500ms)	T_{500}		400	500	650	ms
LOW-level output pulsewidth[4] (800ms)	T_{800}		700	800	900	ms
Noise rejection ratio[5]	S/N		–	–	9	dB

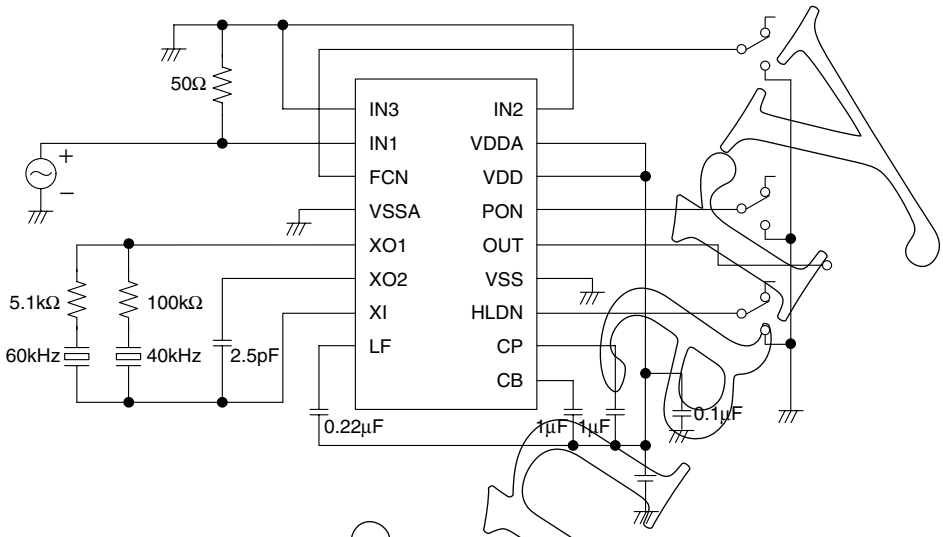
1. Measured using the standard circuit.
2. The time taken under stable wave input conditions from when power is applied or standby is released, using PON, until stable digital output occurs within ratings.
3. The time taken, with 10:1 input signal amplitude ratio and 500ms pulsewidth, from when a change in signal input occurs until the output OUT changes. Note that this characteristic is very dependent on the antenna and crystal filter characteristics. The standard crystal used here has the following equivalent circuit coefficients.



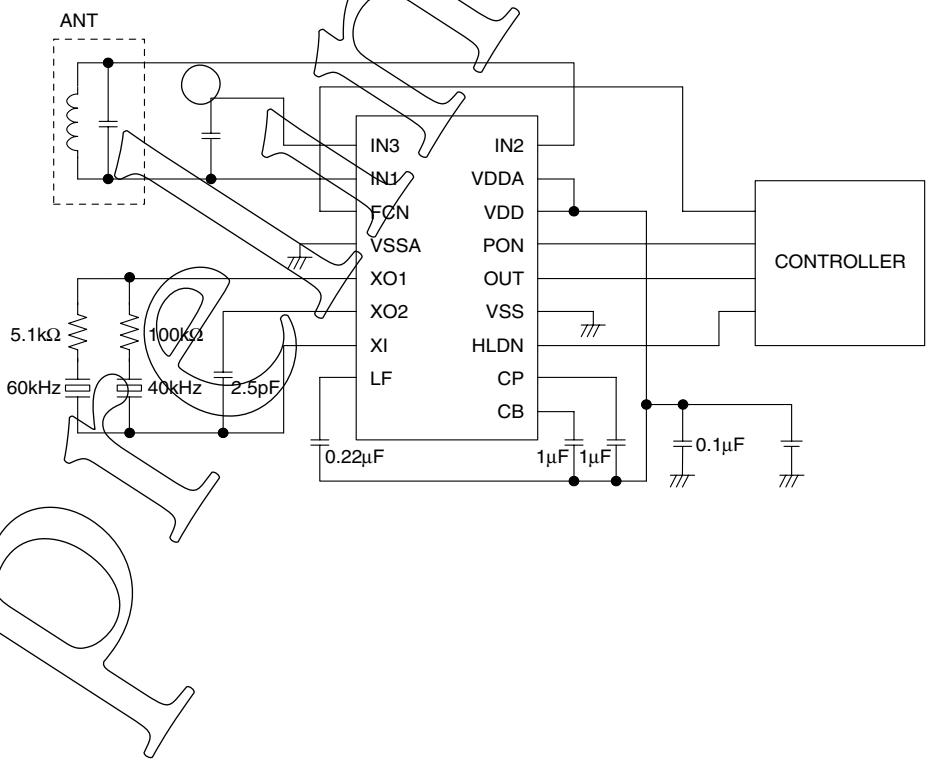
f [kHz]	L1 [kH]	C1 [fF]	R1 [kΩ]	C0 [pF]
40	9.87925	1.60247	33.23400	1.44082
60	6.50427	1.08179	26.94010	1.30860

4. Values obtained when using the standard crystal employed here. Note that these values are dependent on the crystal characteristics, and should be considered as reference values.
5. Time averaged rms values, where the noise is white noise and the measurement bandwidth is determined by the crystal filter equivalent used in the standard circuit.

STANDARD CIRCUIT

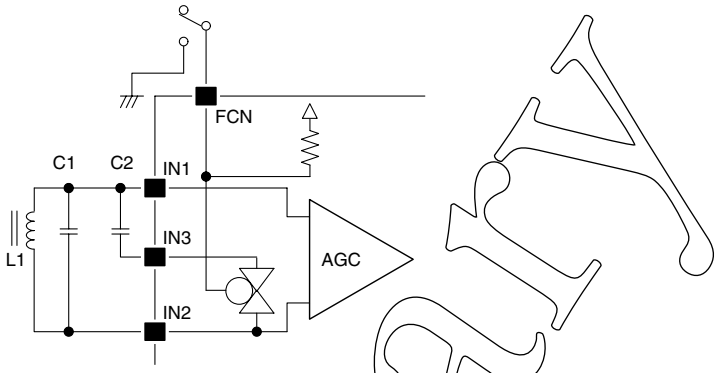


TYPICAL APPLICATION CIRCUIT



FUNCTIONAL DESCRIPTION

Antenna Input and Tuning Capacitor Switching Function



There are three antenna inputs: IN1, IN2, and IN3. When FCN is open (or HIGH), the internal analog switch is OFF and IN1–IN2 are the antenna inputs (60kHz mode). When FCN is LOW, the analog switch is ON, connecting IN3 and IN2. C2 is then connected in parallel to C1 in the tuning circuit, reducing the resonant frequency (40kHz mode).

FCN	Analog switch	Antenna input	Tuning capacitor	Receiver frequency
Open or HIGH	OFF	Between IN1 and IN2	C1	60kHz
LOW	ON	Between IN1 and IN2, IN3	C1 + C2 parallel	40kHz

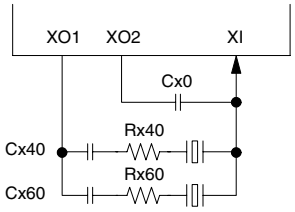
FCN should be left open if not using the tuning capacitor switching function, and IN2 should be connected to IN3 externally.

AGC Amplifier and Gain Hold Function

The input voltage from the antenna is amplified by the AGC amplifier. The gain can be monitored by the voltage on pin CP, and can be changed by varying the CP voltage. An external capacitor Cp can be connected to CP to stabilize the voltage, but the gain tracking time is dependent on the capacitance. When HLDN is open (or HIGH), the gain automatically adjusts to follow the post-amplifier detector signal. When HLDN is LOW, the immediately preceding gain is held for an interval determined by the Cp capacitance.

HLDN	Gain tracking
Open or HIGH	Auto tracking
LOW	Gain held fixed

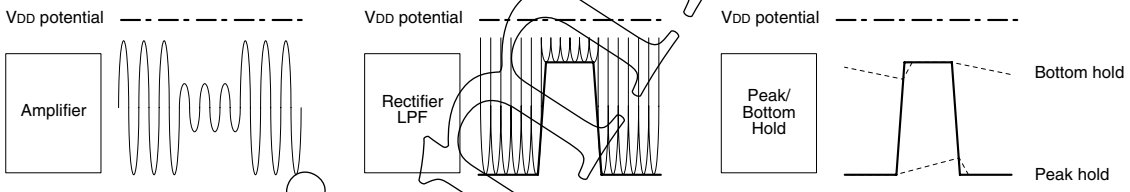
Crystal Filter Circuit



Externally connected crystals are used to form filters. Multiple frequencies (40kHz and 60kHz) are supported by connecting crystals with corresponding frequencies in parallel. The passband center frequency and bandwidth are determined by the crystal characteristics. If the center frequency is lower than the target frequency, capacitors C×40 and C×60 can be connected to adjust the resonant frequency. If the crystal filter Q is high and output delay is large, resistors R×40 and R×60 can be connected to adjust the crystal filter Q factor. An external capacitor C×0 can be connected between XO2 and XI to cancel out the high-frequency components passing through the crystal parallel capacitances. An internal capacitor (3.25pF maximum) is incorporated in the master slice.

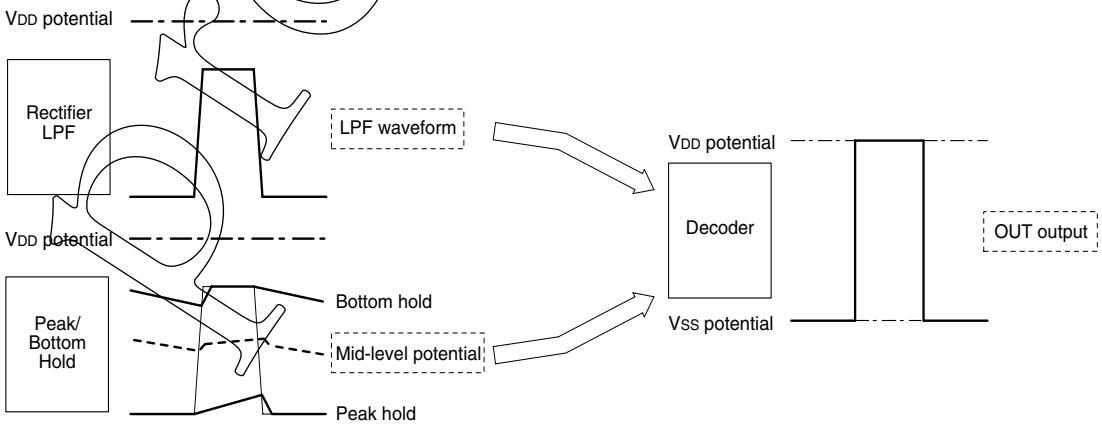
Detector Circuit

The amplified signal is full-wave rectified and passed through a lowpass filter detector. The detector output is input to peak hold (pin CP) and bottom hold (pin CB) circuits to form the decoder reference potentials and peak hold potential for AGC control.



Decoder Circuit

The detector output and peak/bottom hold mid-level potential reference are used to decode the time code signal, which is output on pin OUT. The output is active-LOW, so that the output is LOW when the input amplitude is HIGH.



Standby Function

When PON is open (or HIGH), the device is in standby mode and the current consumption is reduced. Receiver operation starts when PON goes LOW.

PON	Mode	OUT
Open (or HIGH)	Standby	HIGH
LOW	Operating	Time code

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NPC
NIPPON PRECISION CIRCUITS INC.

NIPPON PRECISION CIRCUITS INC.

4-3, Fukuzumi 2-chome, Koto-ku,
Tokyo 135-8430, Japan
Telephone: +81-3-3642-6661
Facsimile: +81-3-3642-6698
http://www.npc.co.jp/
Email: sales@npc.co.jp

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