

OVERVIEW

The SM9503A is a BiCMOS IC RCC*¹ receiver IC. It accepts low frequency standard wave received from an external antenna, amplifies it, detects the data signal, and outputs a digital time code signal.

*¹: Radio controlled clock

FEATURES

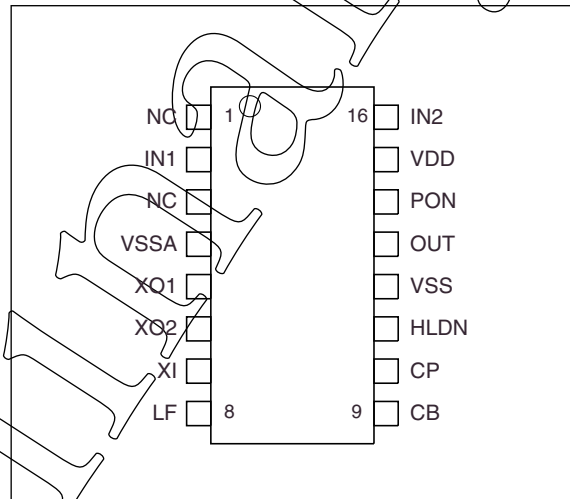
- Operating supply voltage range: 1.2 to 3.6V
- Operating current consumption: 36μA (typ) @ 1.5V
- Standby current consumption: 0.1μA (max) @ 1.5V
- High sensitivity: 0.3μVrms (typ) input @60kHz input
- Low frequency standard wave range: 35kHz to 80kHz
- AGC gain hold function
- External crystal filter connection
- Some versions by a compensation capacitor to cancel the crystal parallel capacitor
- BiCMOS process
- Package: 16-pin VSOP, Chip form

ORDERING INFORMATION

Device	Package
SM9503AV	16-pin VSOP
CF9503A	Chip form

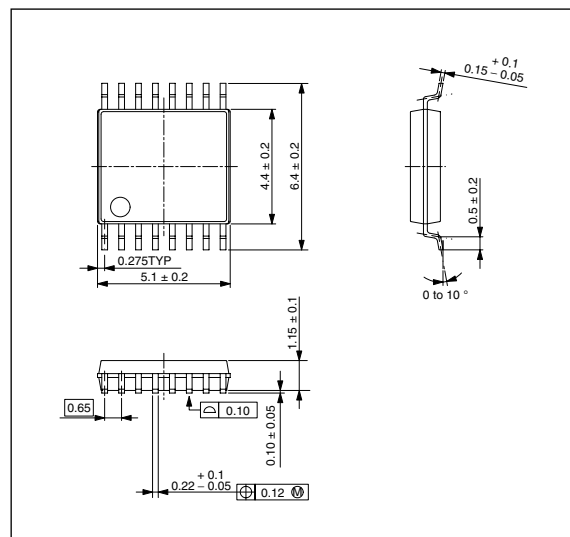
PINOUT

(Top view)



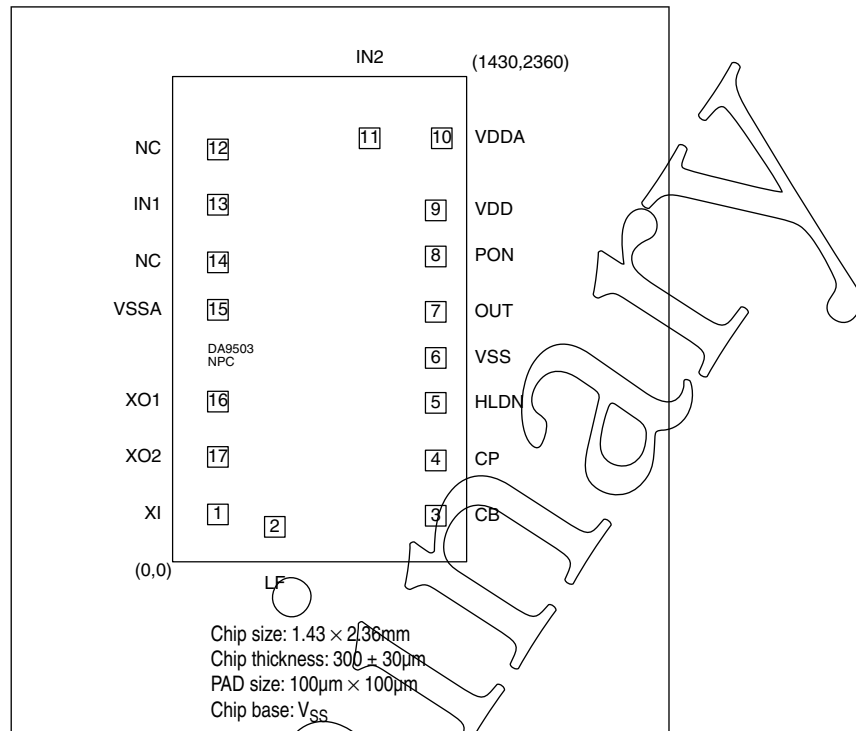
PACKAGE DIMENSIONS

(Unit: mm)



PAD LAYOUT (CF9503A)

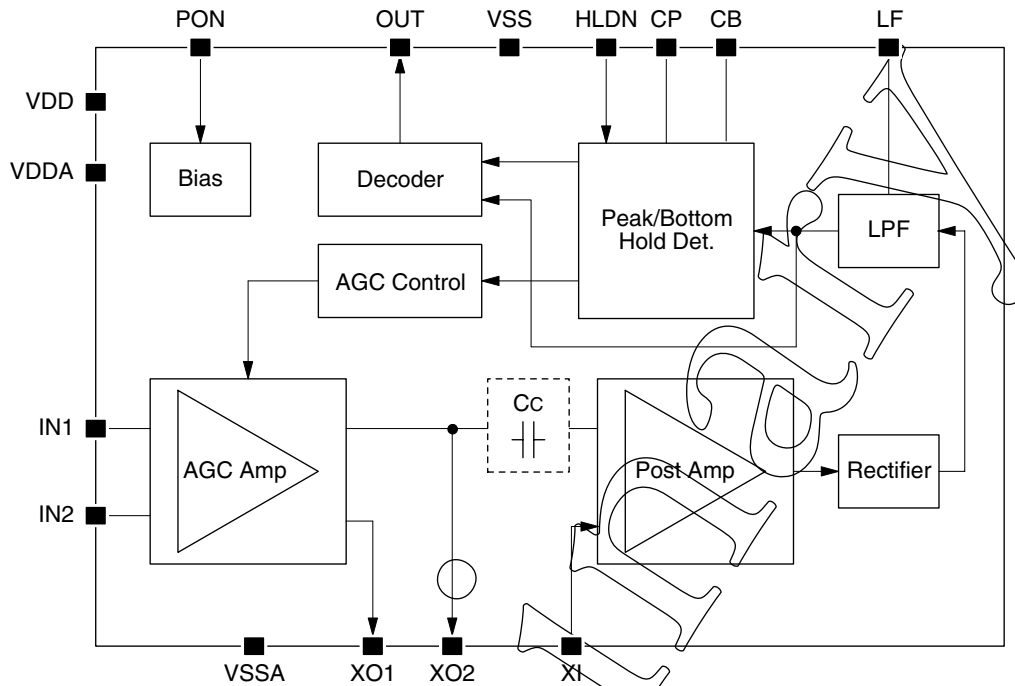
(Unit: μm)



PAD NAME and DIMENSIONS (CF9503A)

Pad number	Pad name	Pad dimensions [μm]	
		X	Y
1	XI	170	280.6
2	LF	447.5	220
3	CB	1230	274.2
4	CP	1230	543.2
5	HLDN	1230	823.4
6	VSS	1230	1042
7	OUT	1230	1266.2
8	PON	1230	1535.2
9	VDD	1230	1759.4
10	VDDA	1259.4	2110
11	IN2	908.4	2110
12	NC	170	2055.8
13	IN1	170	1786.8
14	NC	170	1506.6
15	VSSA	170	1276
16	XO1	170	829.8
17	XO2	170	560.8

BLOCK DIAGRAM



PIN DESCRIPTION

Pad number	Pin number	Name	I/O ¹	A/D ²	Description
1	7	XI	I	A	Crystal filter input connection
2	8	LF	O	A	Rectifier LPF capacitor connection
3	9	CB	O	A	Bottom-hold detector capacitor connection
4	10	CP	O	A	Peak-hold detector capacitor connection
5	11	HLDN	Ipu	D	AGC gain hold control (active LOW)
6	12	VSS	-	A	(-) Negative supply input (substrate potential)
7	13	OUT	O	D	Time code output (active LOW)
8	14	PON	Ipu	D	Standby-mode control input (active LOW)
9	15	VDD	-	A	(+) Positive supply input
10	-	VDDA	-	A	(+) Positive supply input (AGC amplifier)
11	16	IN2	I	A	Antenna input 2
12	1	NC	×	×	No connection (must be open)
13	2	IN1	I	A	Antenna input 1
14	3	NC	×	×	No connection (must be open)
15	4	VSSA	-	A	(-) Negative supply input (AGC amplifier)
16	5	XO1	O	A	Crystal filter output 1
17	6	XO2	O	A	Crystal filter output 2

1. I: input, O: output, Ipu: input with pull-up resistor, -: supply pin
 2. A: analog signal, D: digital signal

SPECIFICATIONS**Absolute Maximum Ratings** $V_{SS} = 0V$

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	V_{DD}		-0.3 to 7.0	V
Input voltage range	V_{IN}		-0.3 to $V_{DD} + 0.3$	V
Power dissipation	P_D	16-pin VSOP	150	mW
Storage temperature range	T_{stg}	16-pin VSOP	-55 to 125	°C
		Chip form	-65 to 150	°C

Recommended Operating Conditions $V_{SS} = 0V$

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	V_{DD}		1.2 to 3.6	V
Operating temperature range	T_{opr}		-20 to 70	°C

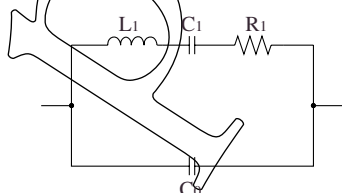
Preliminary

Electrical Characteristics

$V_{DD} = 1.2$ to $3.6V$, $V_{SS} = 0V$, $T_a = -20$ to $70^{\circ}C$ unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Operating supply voltage	V_{DD}		1.2	-	3.6	V
Maximum operating current consumption ¹	I_{DDM}	$V_{DD} = 1.5V$, $T_a = 25^{\circ}C$, no input signal, PON: V_{SS} , OUT: Open	-	50	80	μA
Normal operating current consumption ¹	I_{DDT}	$V_{DD} = 1.5V$, $T_a = 25^{\circ}C$, 0.1mVrms input amplitude (differential input), 500ms pulsewidth, PON: V_{SS} , OUT: Open	-	36	-	μA
Standby mode current consumption	I_{ST}	PON, HLDN: V_{DD} or Open	-	-	0.1	μA
Minimum input voltage range	V_{FMIN}	IN1-IN2 differential input, $F_{IN} = 60kHz$	-	0.3	1.0	μV_{rms}
Maximum input voltage range	V_{FMAX}	IN1-IN2 differential input, $F_{IN} = 60kHz$	80	-	-	mVrms
Input frequency	F_{IN}	IN1-IN2 differential input	35	-	80	kHz
Startup time ²	t_{ON}	When supply is applied	-	-	8	sec
Startup time (PON) ²	t_{PON}	From standby mode	-	-	8	sec
Input voltage	V_{IL}	PON, HLDN	-	-	0.2	V
	V_{IH}	PON, HLDN	$V_{DD} - 0.2$	-	-	V
Input current	I_{IL}	$V_{IN} = 0V$, PON, HLDN	-1	-	-	μA
	I_{IH}	$V_{IN} = V_{DD}$, PON, HLDN	-	-	1	μA
Output voltage	V_{OL}	$I_{OL} = 5\mu A$, OUT	-	-	0.2	V
	V_{OH}	$I_{OH} = -5\mu A$, OUT	$V_{DD} - 0.2$	-	-	V
Gain hold time	t_{HLD}	$\leq \pm 3dB$ variation	1	-	-	sec
Fall time output propagation delay ³	t_{DN}		-	-	160	ms
Rise time output propagation delay ³	t_{UP}		-	-	200	ms
LOW-level output pulsewidth ⁴ (200ms)	T_{200}		100	200	300	ms
LOW-level output pulsewidth ⁴ (500ms)	T_{500}	$F_{IN} = 60kHz$, NPC standard crystal, NPC standard jig	400	500	650	ms
LOW-level output pulsewidth ⁴ (800ms)	T_{800}		TBD	800	TBD	ms
LOW-level output pulsewidth ⁴ (900ms)	T_{900}		TBD	900	TBD	ms
Noise rejection ratio ⁵	S/N		-	-	9	dB

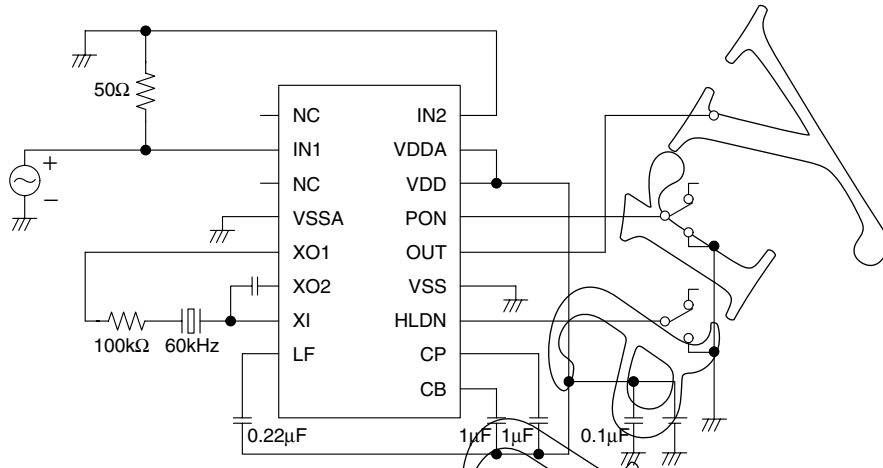
1. Measured using the standard circuit.
2. The time taken under stable wave input conditions from when power is applied or standby is released, using PON, until stable digital output occurs within ratings.
3. The time taken, with 10:1 input signal amplitude ratio and 500ms pulsewidth, from when a change in signal input occurs until the output OUT changes. Note that this characteristic is very dependent on the antenna and crystal filter characteristics. The standard crystal used here has the following equivalent circuit coefficients.



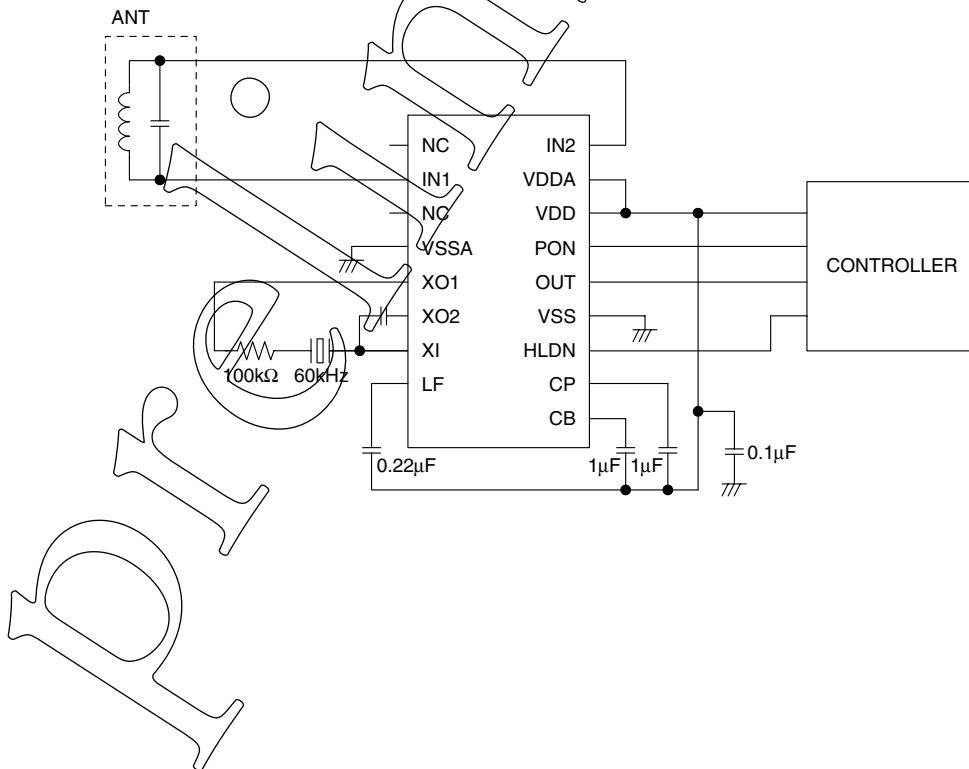
f [kHz]	L1 [kH]	C1 [fF]	R1 [kΩ]	C0 [pF]
60	TBD	TBD	TBD	TBD

4. Values obtained when using the NPC standard crystal employed here. Note that these values are dependent on the crystal characteristics, and should be considered as reference values.
5. Time averaged rms values, where the noise is white noise and the measurement bandwidth is determined by the crystal filter equivalent used in the standard circuit.

STANDARD CIRCUIT



TYPICAL APPLICATION CIRCUIT



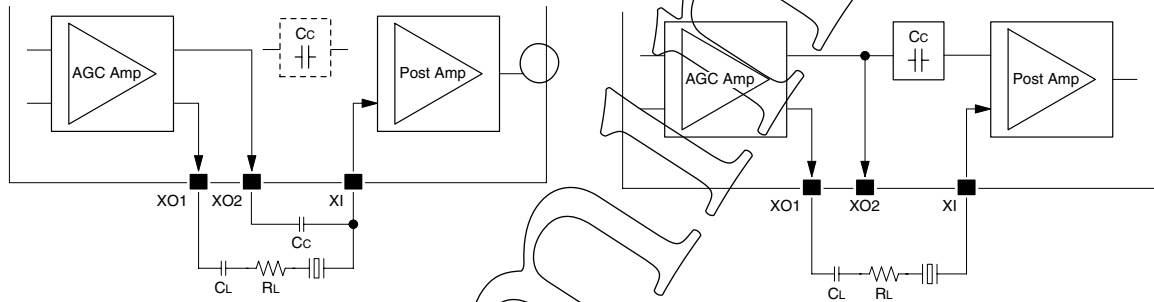
FUNCTIONAL DESCRIPTION

AGC Amplifier and Gain Hold Function

The input voltage from the antenna is amplified by the AGC amplifier. The gain can be monitored by the voltage on pin CP, and can be changed by varying the CP voltage. An external capacitor C_p can be connected to CP to stabilize the voltage, but the gain tracking time is dependent on the capacitance. When HLDN is open (or HIGH), the gain automatically adjusts to follow the post-amplifier detector signal. When HLDN is LOW, the immediately preceding gain is held for an interval determined by the C_p capacitance.

Crystal Filter Circuit

External crystals are used as filters. The center frequency and bandwidth of the filters is determined by the crystal characteristics. If the center frequency is lower than the target frequency, it is necessary to add C_L capacitor for the adjustment frequency. If Q of the crystal filter is higher and the output delay is larger, it is necessary to add R_L to adjust it. Adding a compensation capacitor C_C , it is possible to select built-in or external, cancels the high-frequency components pass through the crystal parallel capacitance. Compensation capacitors are built in, and wiring them inside makes possible to select versions of the required capacitances from 0.5pF to 2.0pF.

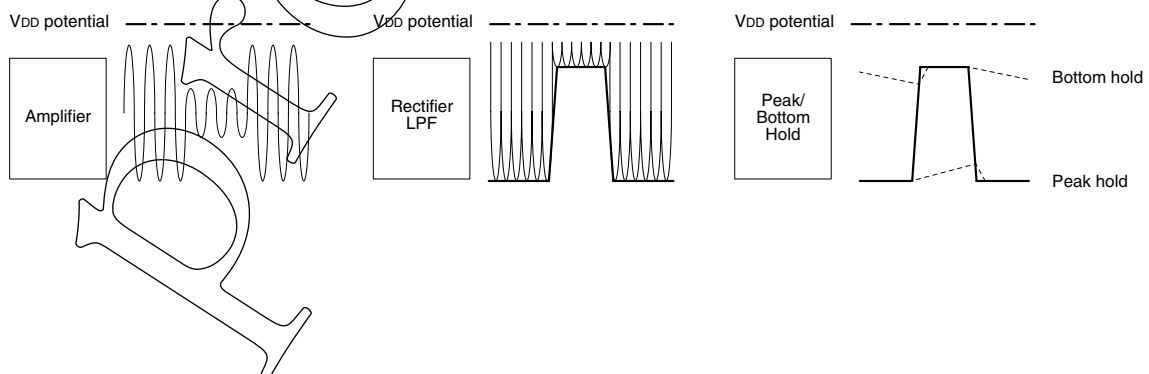


The case of using the external compensation capacitor

The case of using built-in compensation capacitor

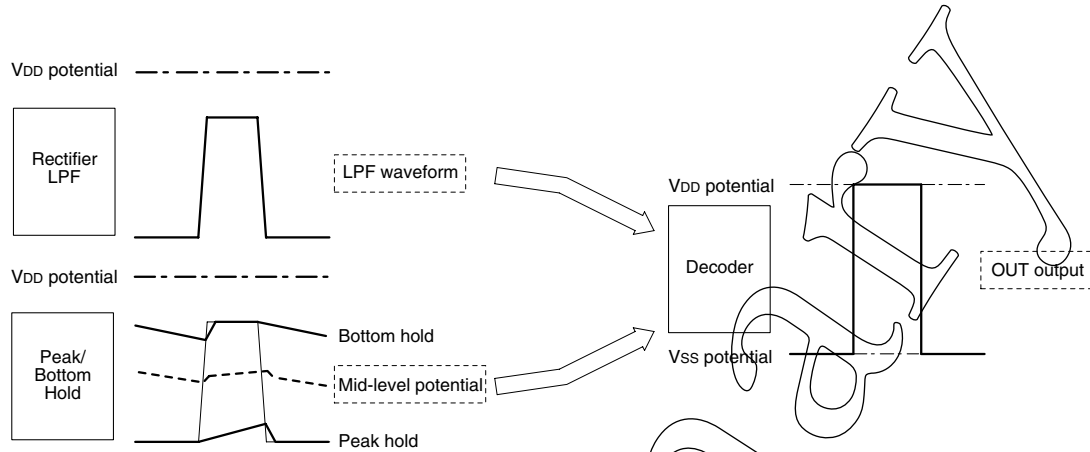
Detector Circuit

The amplified signal is full-wave rectified and passed through a lowpass filter detector. The detector output is input to peak hold (pin CP) and bottom hold (pin CB) circuits to form the decoder reference potentials and peak hold potential for AGC control.



Decoder Circuit

The detector output and peak/bottom hold mid-level potential reference are used to decode the time code signal, which is output on pin OUT. The output is active-LOW, so that the output is LOW when the input amplitude is HIGH.



Standby Function

When PON is open (or HIGH), the device is in standby mode and the current consumption is reduced. Receiver operation starts when PON goes LOW.

PON	Mode	OUT
Open (or HIGH)	Standby	HIGH
LOW	Operating	Time code

Preliminary

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